REMARKS

I. Introduction

Claims 35-75 are pending in the application.

Please cancel, without prejudice, claims 74 and 75.

Applicants note with appreciation that the Examiner has allowed claims 35-51 over the prior art.

Claims 74-75 are rejected under 35 U.S.C. § 102(b) in view of Murdock U.S. Patent 5,243,623 (hereinafter "Murdock").

Claims 52-73 are rejected under 35 U.S.C. § 103(a) in view of Murdock and Pierce et al. U.S. Patent 5,581,199 (hereinafter "Pierce").

Reconsideration of this application in light of the following remarks is respectfully requested.

II. The Rejections Based on 35 U.S.C. § 102(b)

Claims 74 and 75 are rejected under 35 U.S.C. § 102(b) as anticipated by Murdock. Applicants have canceled these claims and therefore respectfully request that this rejection be withdrawn.

III. The Rejections Based on 35 U.S.C. § 103(a)

Claims 52-73 are rejected under 35 U.S.C. § 103(a), as being unpatentable over Murdock in view of Pierce. Applicants respectfully traverse.

The Examiner rejected the above-identified claims contending that Murdock teaches applicants' invention substantially as claimed, with the exception of a plurality of programmable logic elements to select between a first logic standard and a second logic standard. The Examiner contends this element is supplied by Pierce and that it would be obvious to combine these references to produce the claimed invention. Applicants respectfully disagree.

Claims 52-73 are directed towards apparatus that allows an electronic device to select a logic standard from at least one of two available different logic standards and operate at the selected standard. These claims specify that programmable elements are used to select a desired logic standard from several possible logic standards (*e.g.*, by appropriately programming an input or output buffer). One advantage of this arrangement is that it provides an I/O architecture that may be programmably configured by a circuit designer prior to use to function at a preset logic standard. Thus, if an end user needs to connect to external circuitry employing standard CMOS logic, an electronic device that can provide and receive the appropriate drive signals is needed. However, simply changing the external environment to

one that operates at a different logic standard, such as GTL, may require a different electronic device, although the basic device is substantially the same. Applicants' invention solves this problem by providing I/O devices and methods that allow the user to programmably select any one of several different logic standards prior to use, so that a single electronic device is adaptable and may be used with a wide variety of external circuitry that operates at a different logic standards.

The Examiner's proposed combination of Pierce and Murdock fails to show or suggest applicants' claimed invention. For example, the transceiver circuit shown in Murdock relies on external sensing pins to determine whether to function in a differential or single-ended SCSI operating mode (Murdock, column 4, lines 38-50). The purpose of this sensing pin (and the Murdock circuit generally) is to allow the transceiver circuitry to sense input conditions and dynamically adapt to the appropriate mode of operation. This allows an SCSI bus on a personal computer to be connected to numerous peripheral devices such as computer monitors and printers without the user being concerned about whether the peripheral is compatible with the computer (*i.e.*, operates in appropriate single-ended or differential mode). Thus, the purpose of the Murdock transceiver is to provide the flexibility to connect, disconnect, and reconnect to various external components, each of which may operate at an unknown mode (differential or single-ended). Murdock accomplishes this by sensing input conditions and

adjusting the transceiver to operate according to the sensed mode (Murdock, column 2, lines 3-6).

Applicants' claimed invention, however, is not concerned with sensing output conditions to dynamically determine an appropriate mode of operation. Rather, the claims at issue are concerned with the use of programmable logic elements to select a desired one of several available logic standards *prior to use*. This is vastly different from Murdock because the purpose of the Murdock transceiver is to flexibly switch between the two modes of operation within the SCSI standard, depending on what it is connected to (dynamic operation); whereas applicants' claimed invention is concerned with selecting a particular logic standard and remaining in that configuration regardless of changes in external conditions (predefined static operation).

This difference is significant because if the transceiver of Murdock is modified to include the programmable elements of Pierce as the Examiner suggests (Office Action, page 4), it cannot provide the vital mode flexibility feature it is designed for because it would be "stuck" (*i.e.*, statically programmed) to operate in one mode only. So, for example, if a PC user attempted to change to a peripheral operating at a different SCSI mode, the transceiver would not work as intended (that is, it would not change modes), discouraging such a modification. Thus, the Murdock reference teaches away from the static programmablity specified by applicants' claimed invention

and therefore cannot be properly combined with the programmable elements of Pierce as suggested by the Examiner.

Furthermore, applicants point out that the memory cells of Pierce cited by the Examiner for combination with Murdock are not used to select logic standards, but rather to control the slew rate and capacitive/resistive response of an output buffer (Pierce, column 18, lines 57-62). Adjusting these characteristics merely modifies the data rate or provides improved impedance matching to a transmission line. This, however, has absolutely nothing to do with selecting the operating modes or logic standards of a transceiver device. Thus, Pierce fails to recognize the need for or desirability of changing the logic standard of an output buffer, and Murdock teaches away from adding the static programmable elements contained in Pierce. Accordingly, there is no motivation to combine these references as suggested by the Examiner, and in fact, such a combination is expressly discouraged by Murdock.

It is well settled law that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion by the prior art supporting the combination -- to do otherwise would be hindsight reconstruction, which is not permissible. ACS Hosp. Systems, Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed Cir. 1984). Thus, because Pierce and Murdock fail to provide any motivation to combine, and in fact teach away from the Examiner's proposed combination, applicants request that

the obviousness rejection be withdrawn. Accordingly, applicants respectfully submit that claims 52, 62, 71, and the claims that depend therefrom are allowable.

IV. Conclusion

The foregoing demonstrates that claims 52-73 are allowable. Thus, this application is in a condition for allowance. Reconsideration and allowance are therefore respectfully requested.

Respectfully submitted,

Jared Kneitel
Registration No. 51,178
Agent for Applicants
Customer Number 36,981
FISH & NEAVE
1251 Avenue of the Americas
New York, NY 10020-1104
Tel.: (212) 596-9000